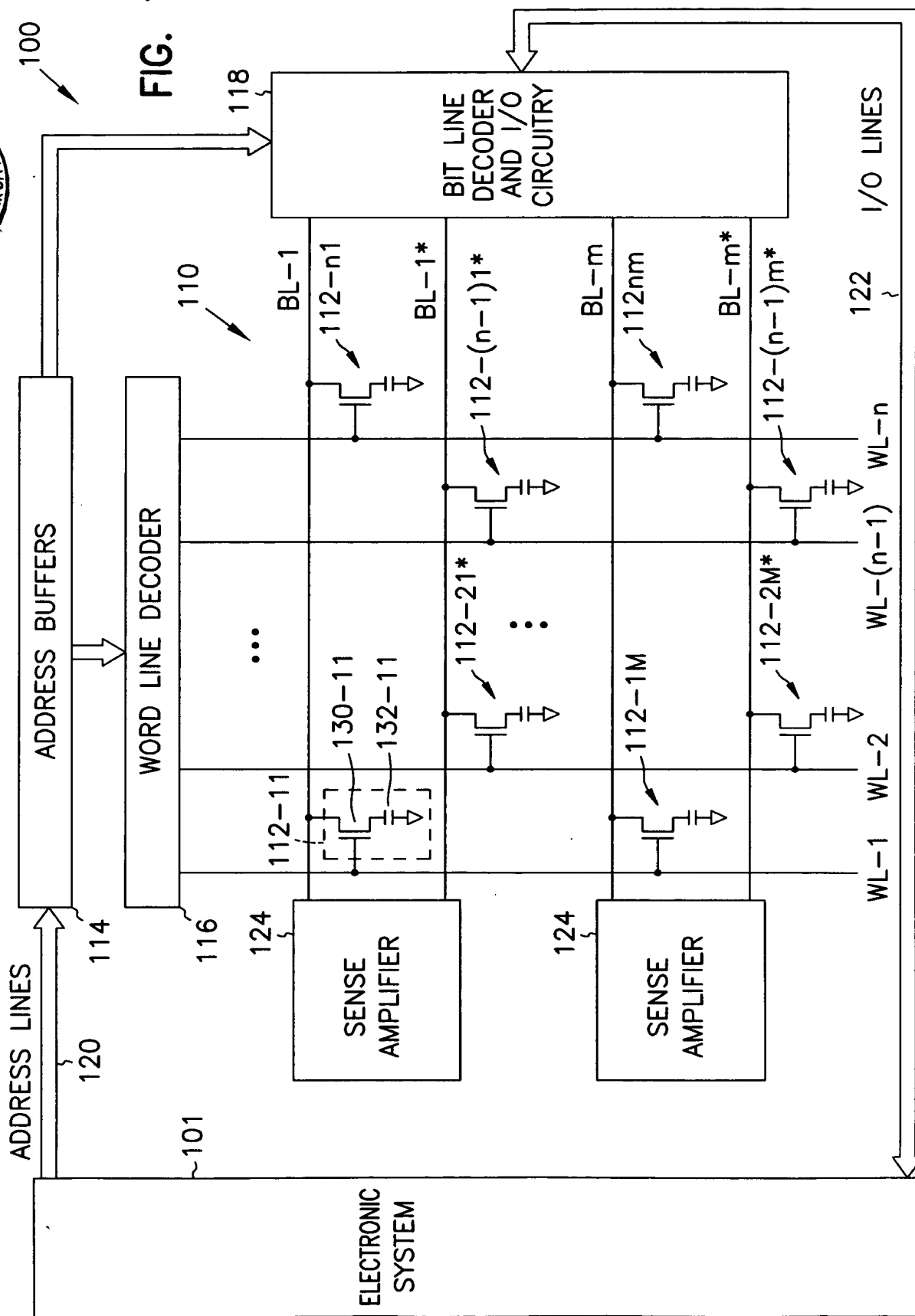


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FIG. 1



TITLE: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL
WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

INVENTORS NAME: Wendell P. Noble Jr. et al.

SERIAL NO.: 09/551,027

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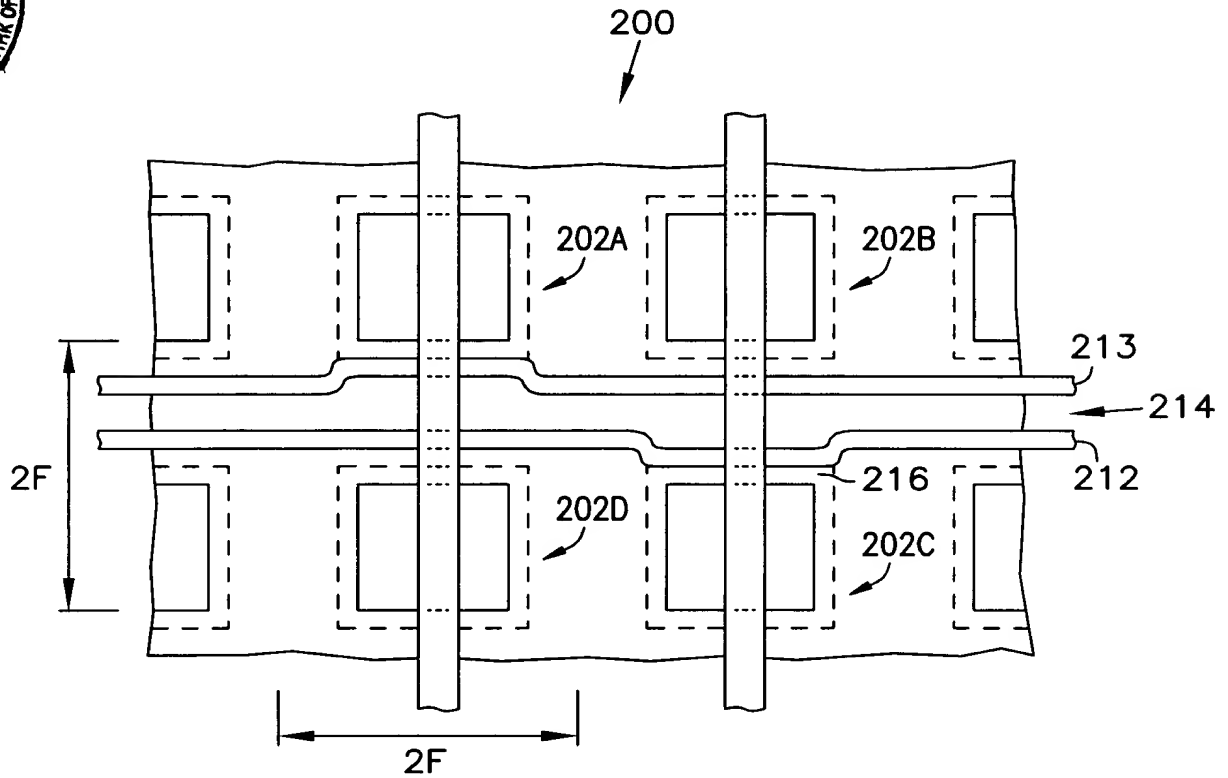


FIG. 2

TITLE: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL
WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

INVENTORS NAME: Wendell P. Noble Jr. et al.

SERIAL NO.: 09/551,027

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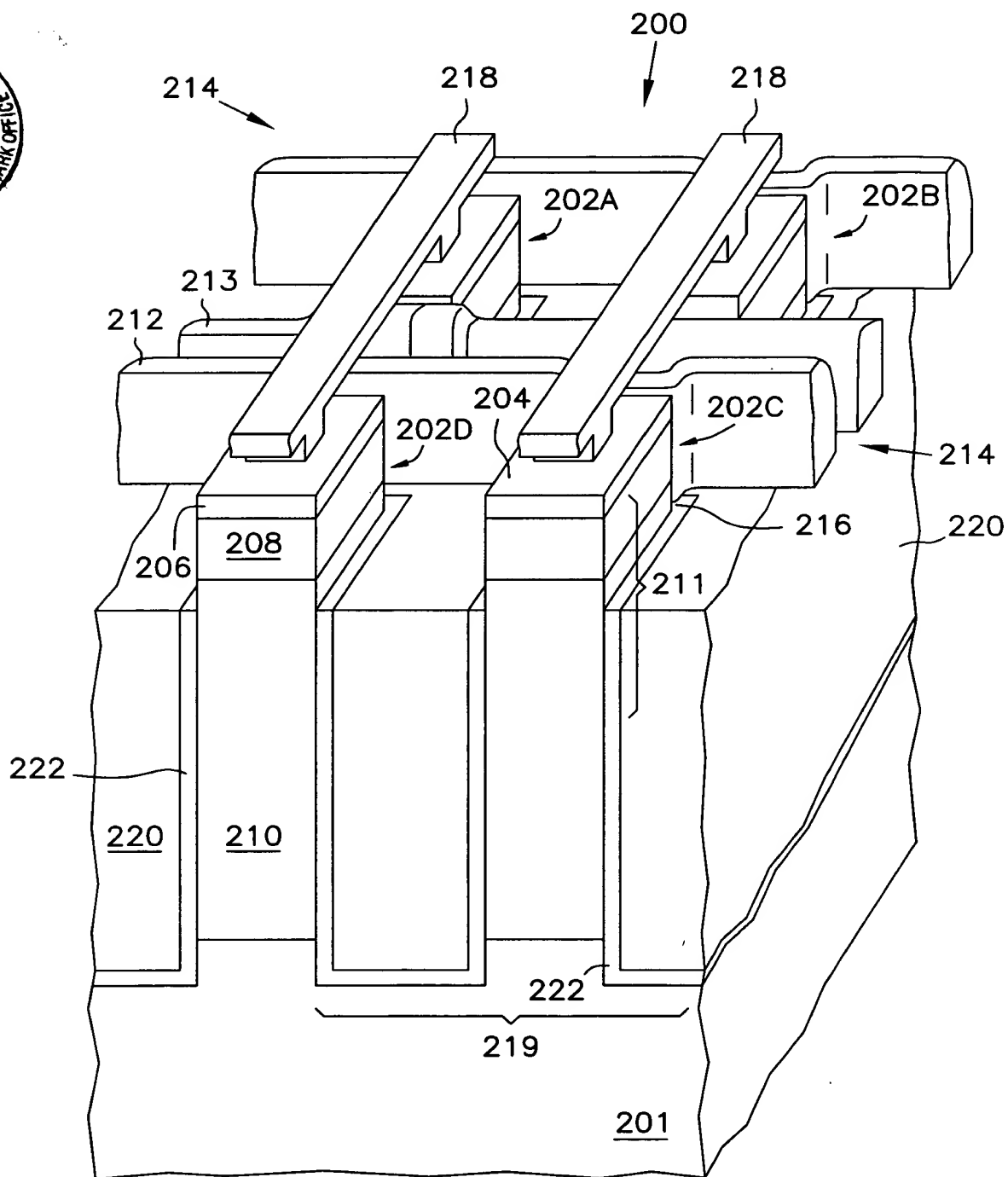


FIG. 3

TITLE: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL
WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

INVENTORS NAME: Wendell P. Noble Jr. et al.

SERIAL NO.: 09/551,027

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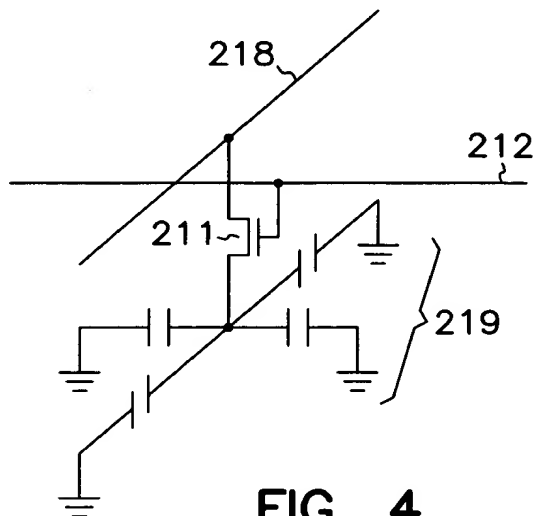
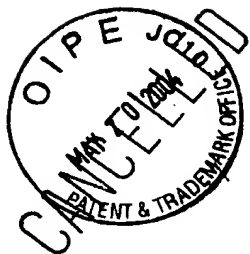


FIG. 4

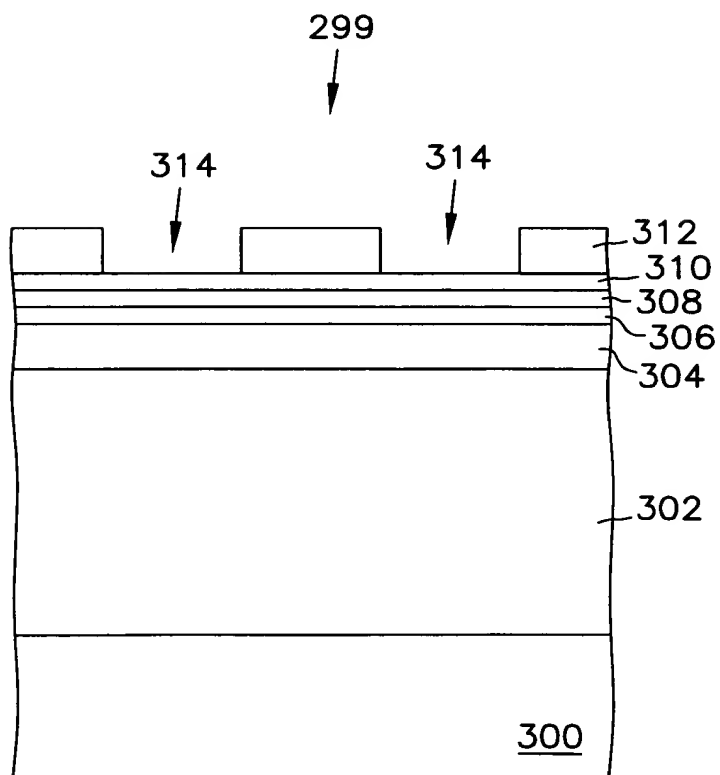


FIG. 5A

TITLE: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL
WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

INVENTORS NAME: Wendell P. Noble Jr. et al.

SERIAL NO.: 09/551,027

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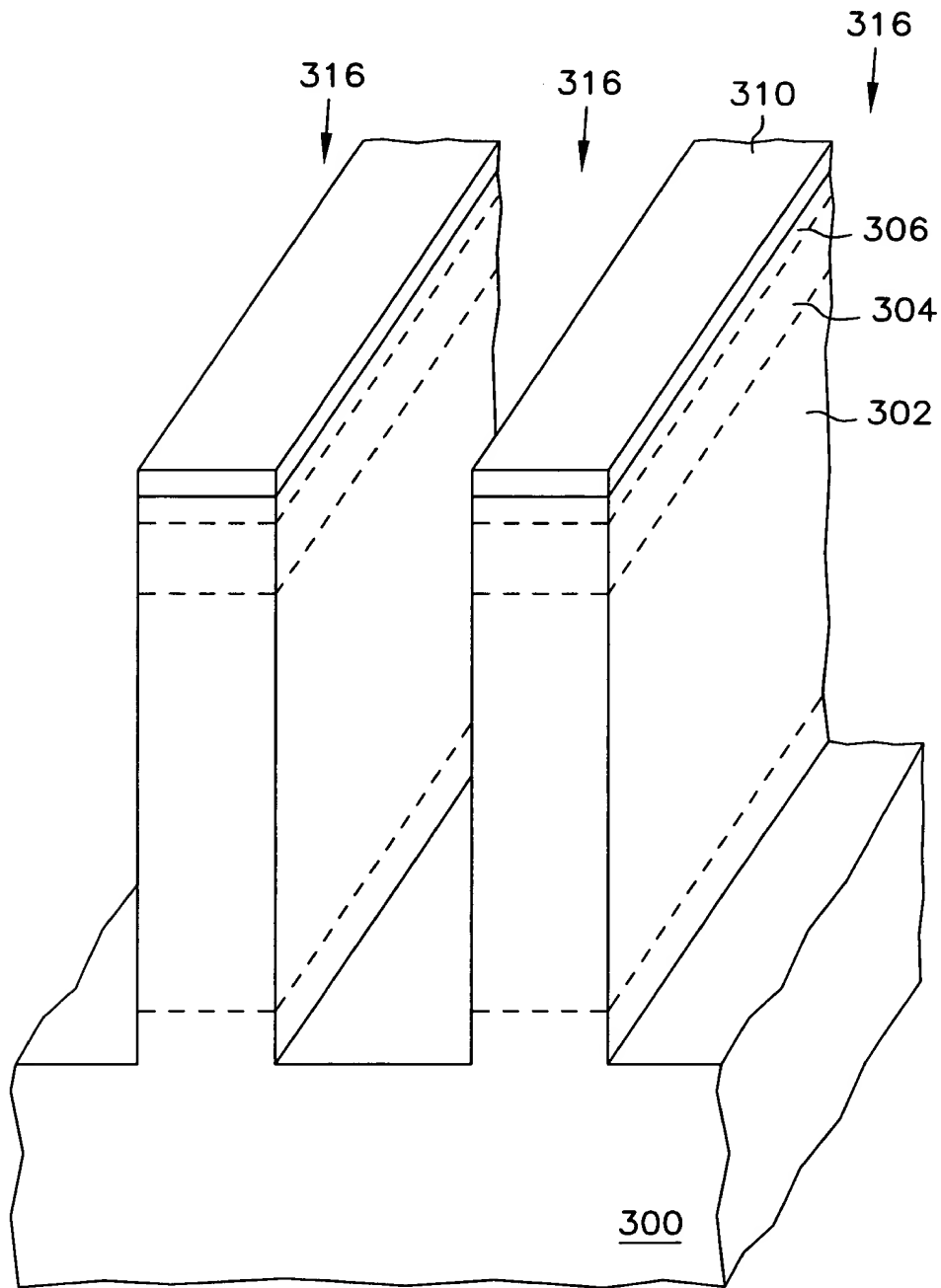
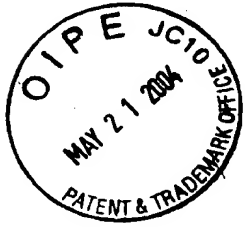


FIG. 5B

TITLE: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL
WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR
INVENTORS NAME: Wendell P. Noble Jr. et al.
SERIAL NO.: 09/551,027

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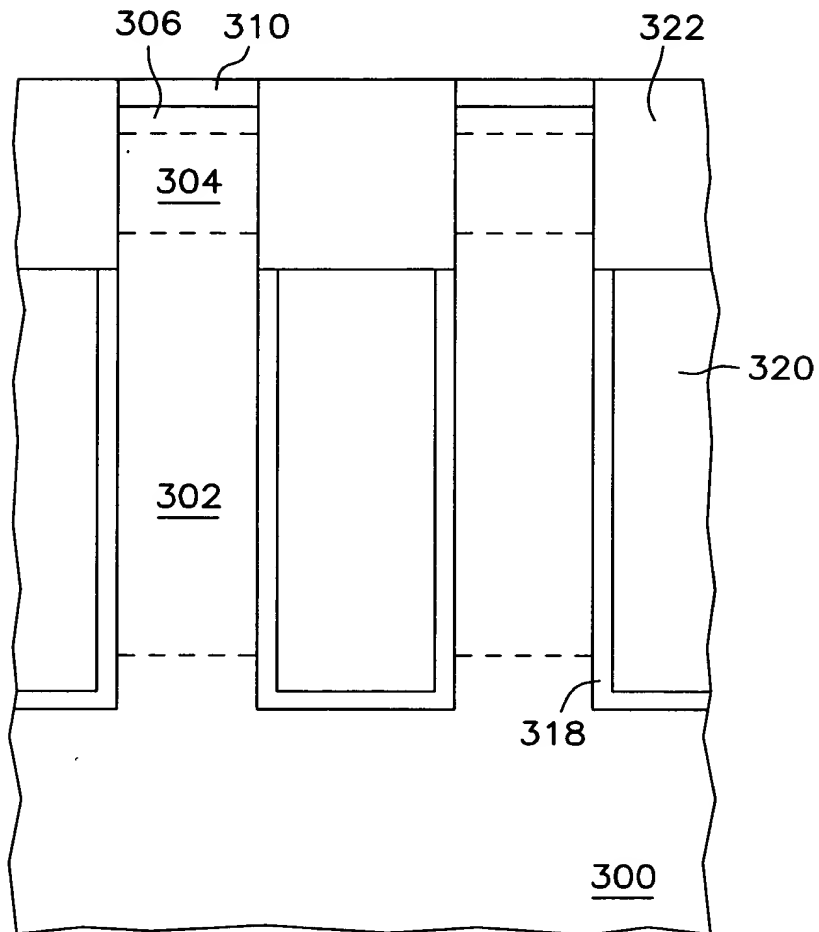
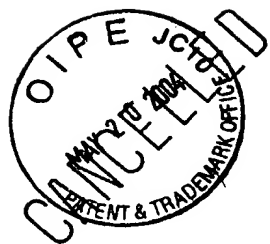


FIG. 5C

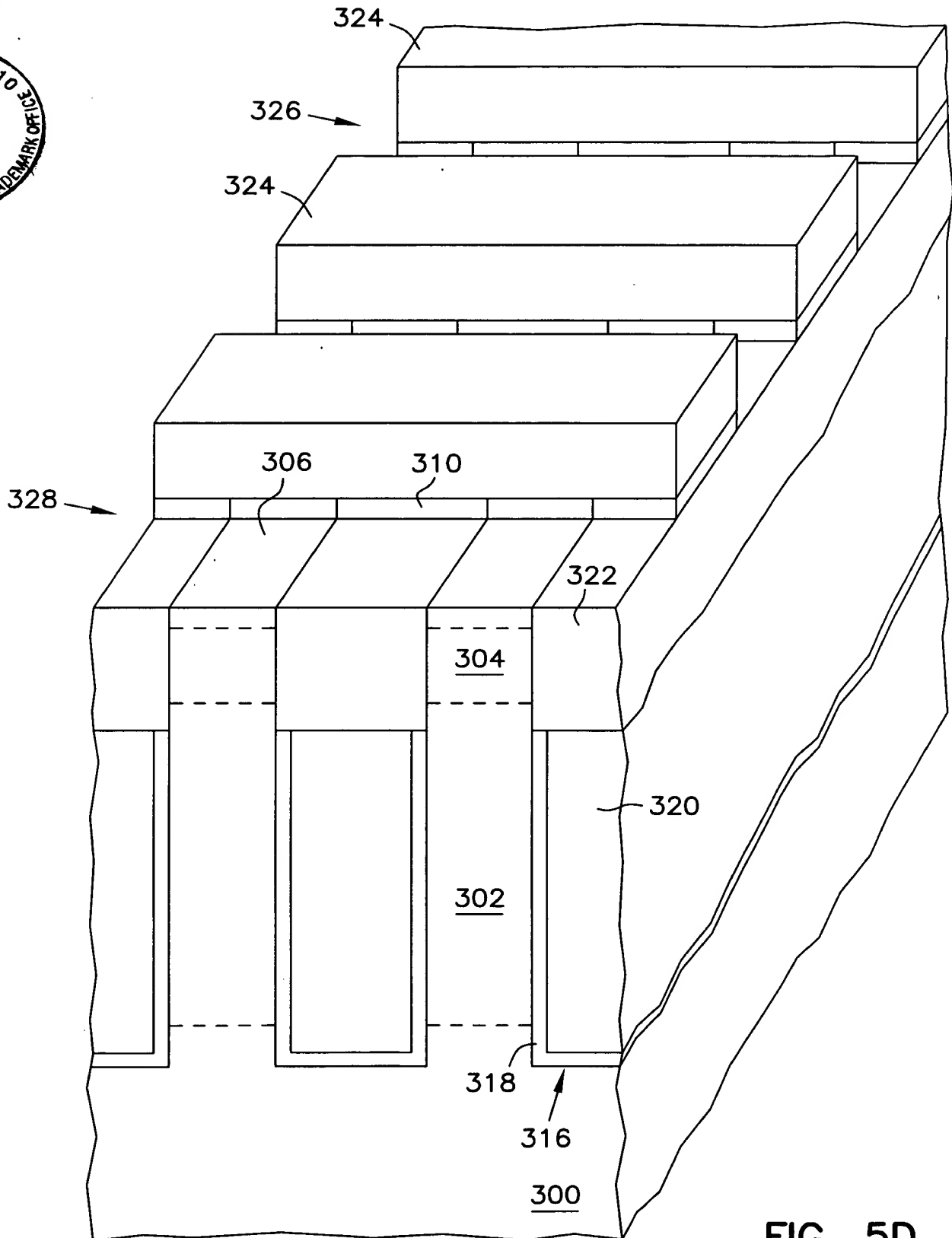
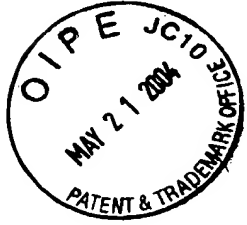
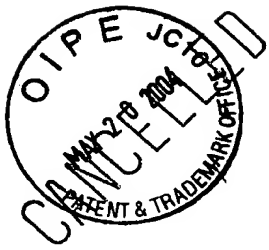


FIG. 5D



TITLE: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL
WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR
INVENTORS NAME: Wendell P. Noble Jr. et al.
SERIAL NO.: 09/551,027

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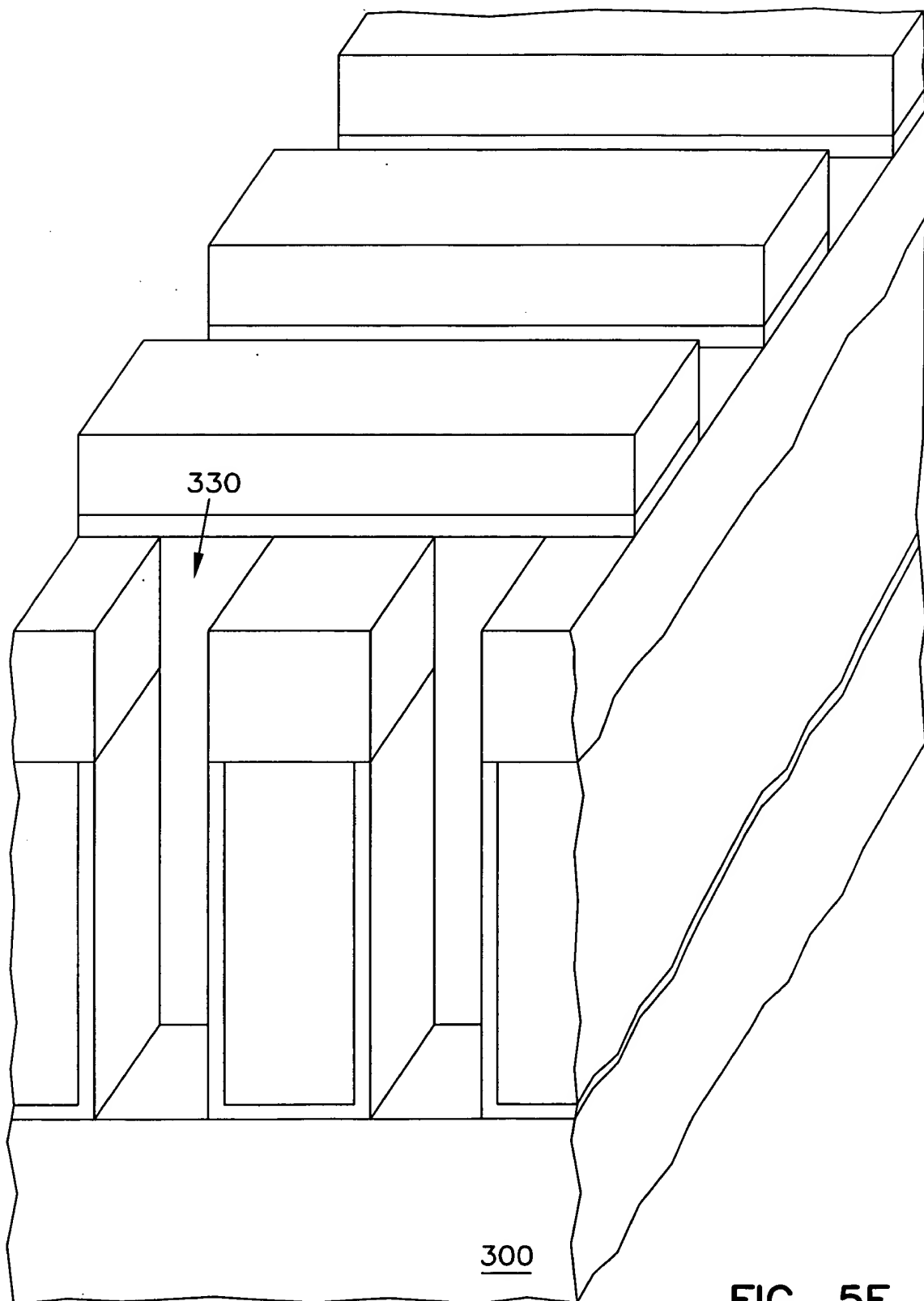
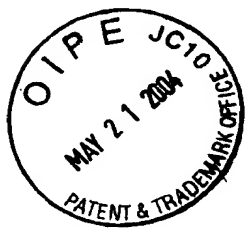


FIG. 5E



TITLE: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL
WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

INVENTORS NAME: Wendell P. Noble Jr. et al.

SERIAL NO.: 09/551,027

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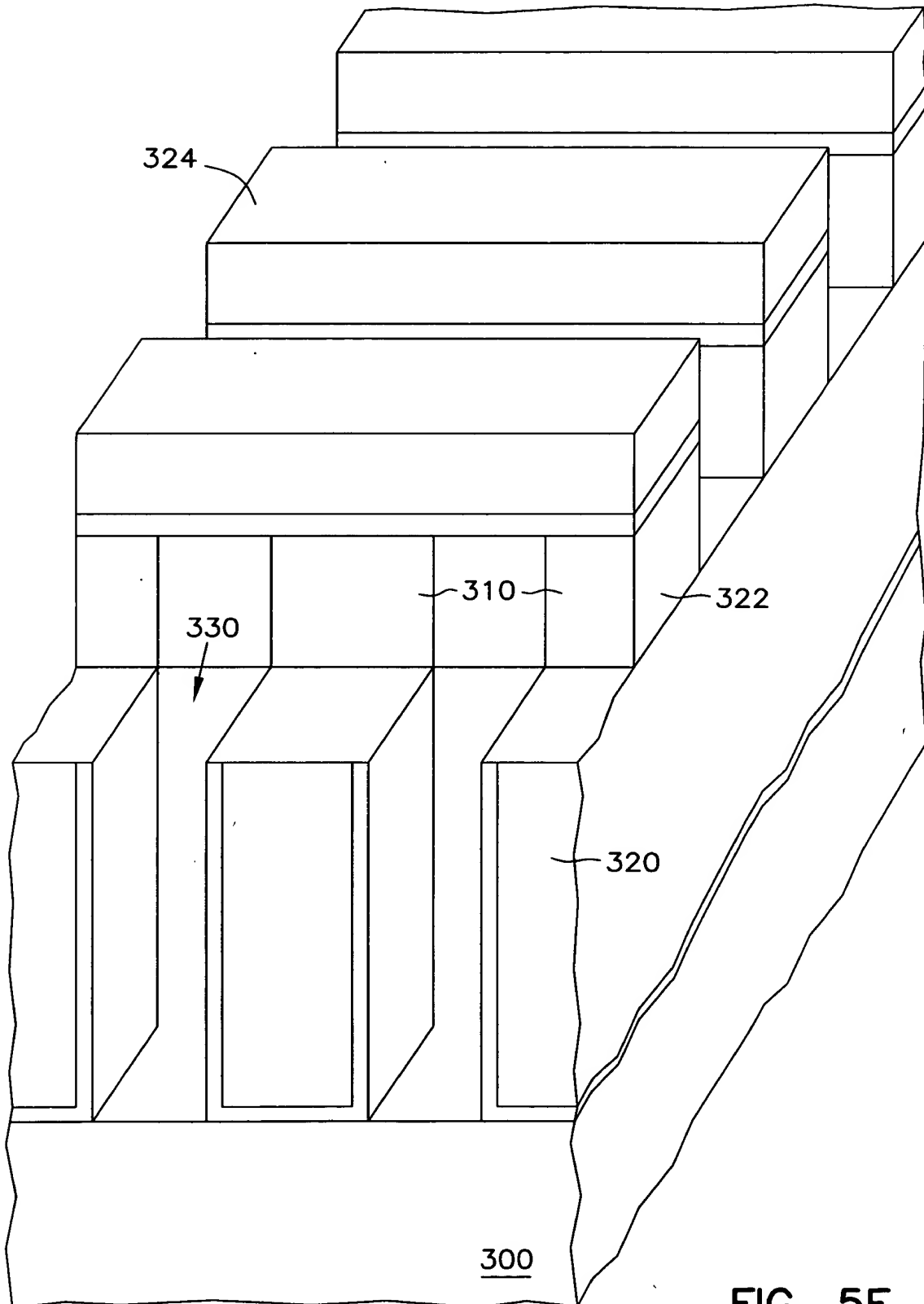


FIG. 5F

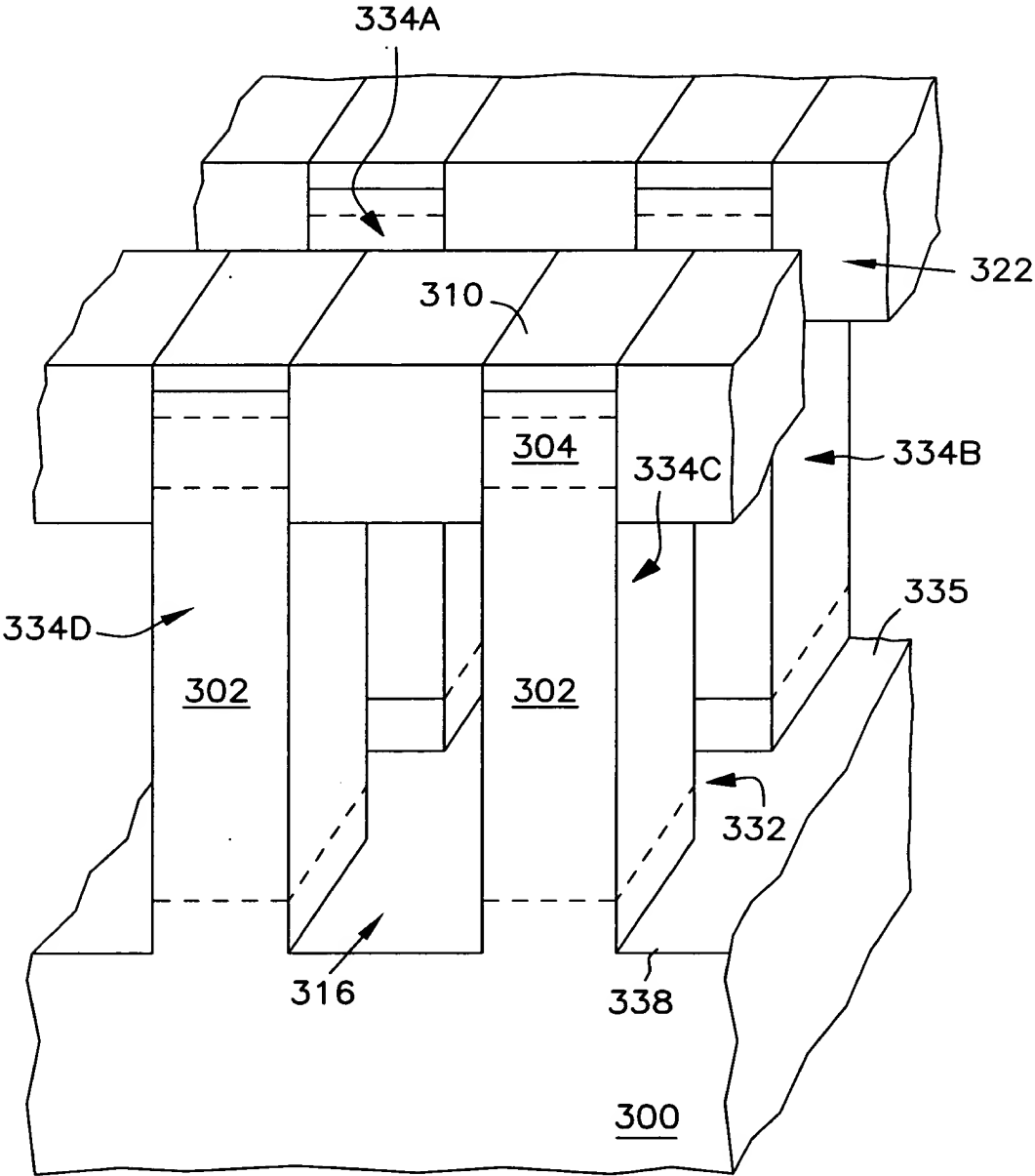
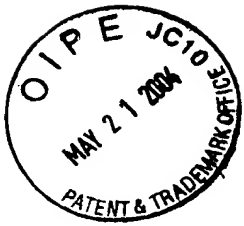


FIG. 5G

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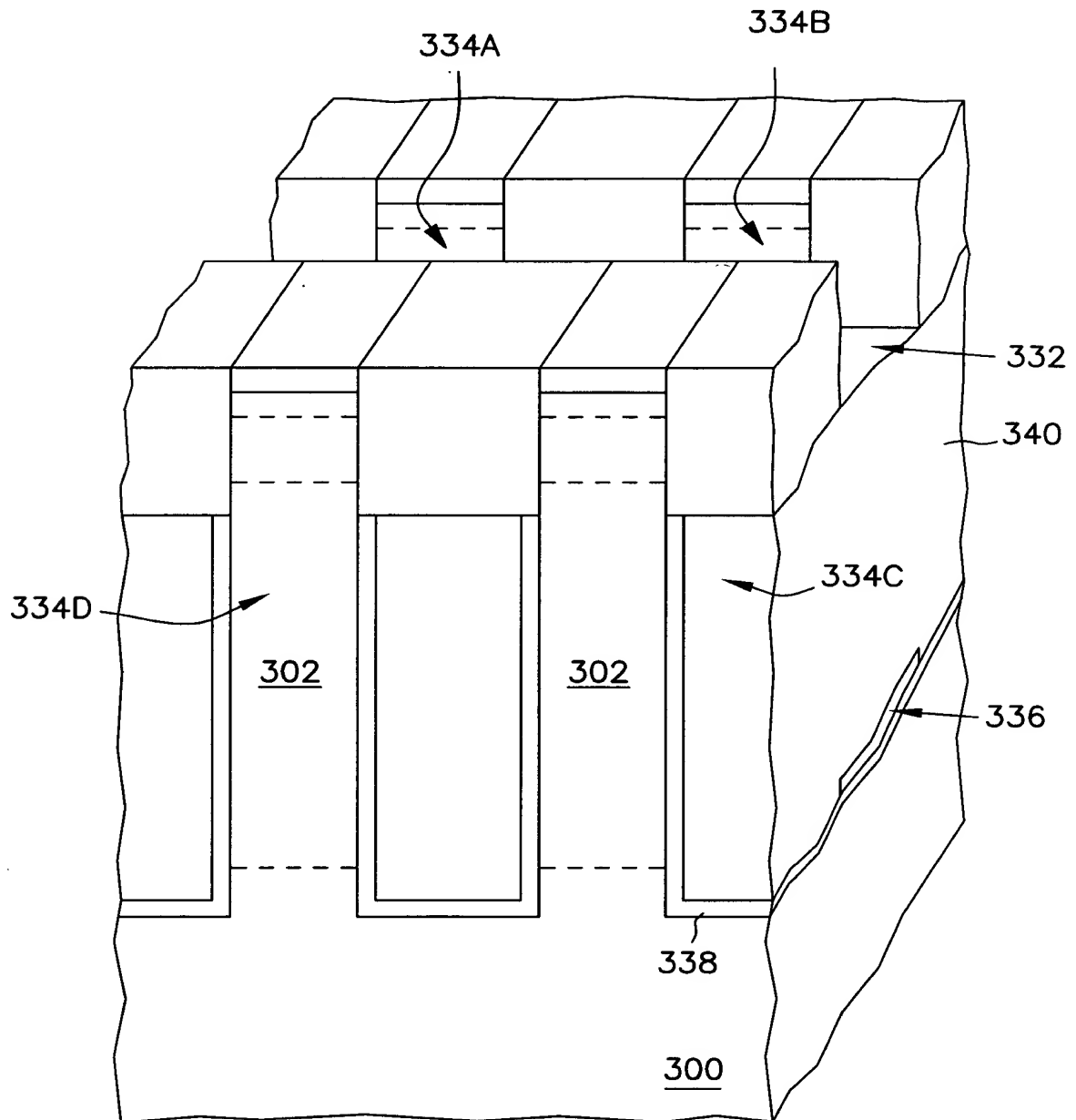
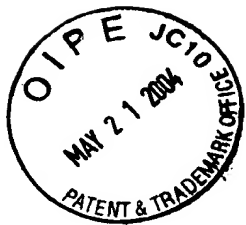


FIG. 5H



TITLE: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL
WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

INVENTORS NAME: Wendell P. Noble Jr. et al.

SERIAL NO.: 09/551,027

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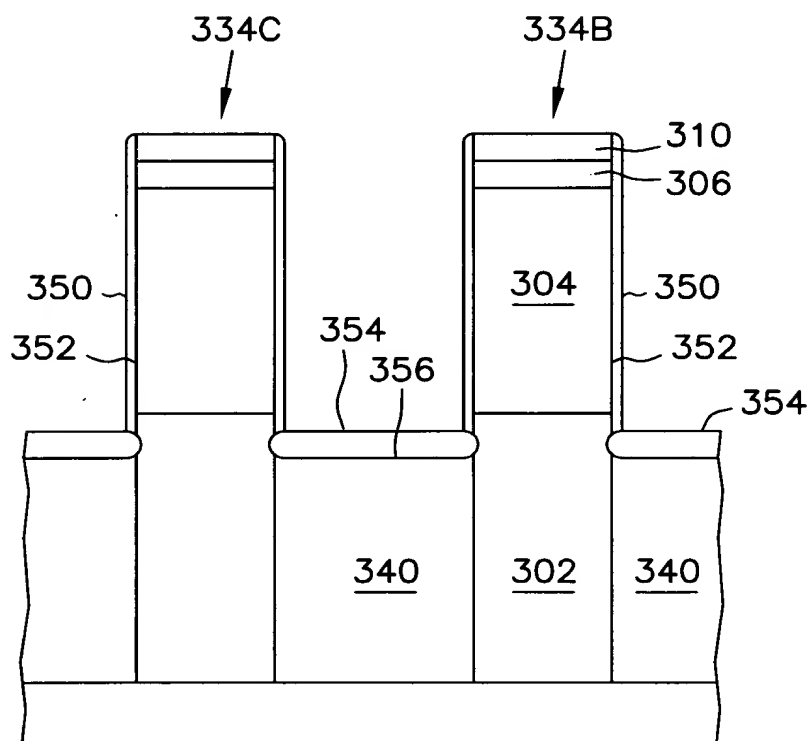


FIG. 5I



TITLE: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL
WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

INVENTORS NAME: Wendell P. Noble Jr. et al.

SERIAL NO.: 09/551,027

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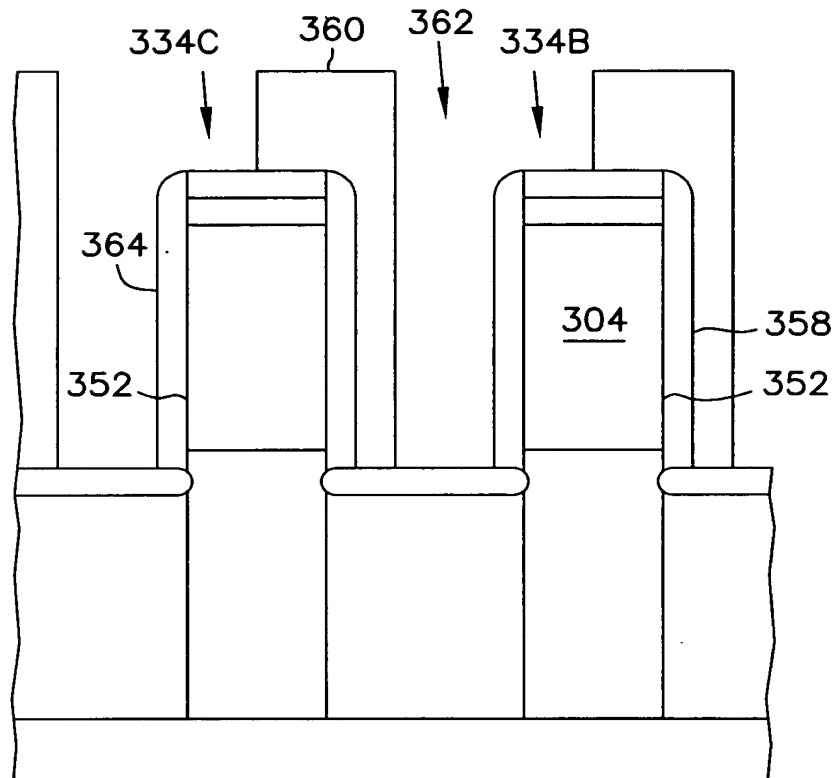
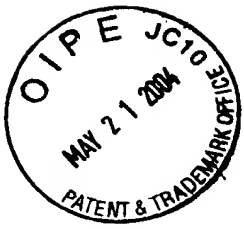


FIG. 5J



TITLE: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL
WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

INVENTORS NAME: Wendell P. Noble Jr. et al.

SERIAL NO.: 09/551,027

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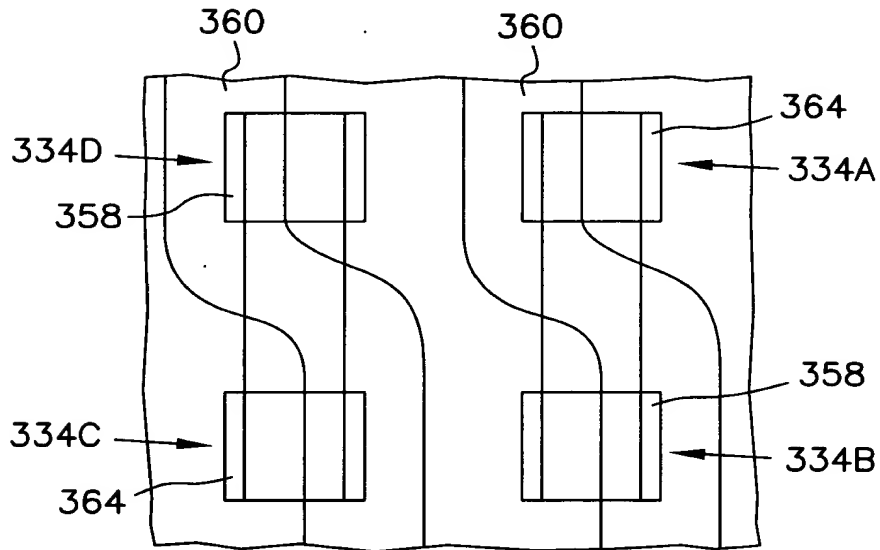
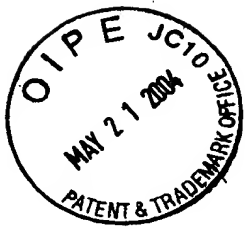


FIG. 5K



TITLE: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL
WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

INVENTORS NAME: Wendell P. Noble Jr. et al.

SERIAL NO.: 09/551,027

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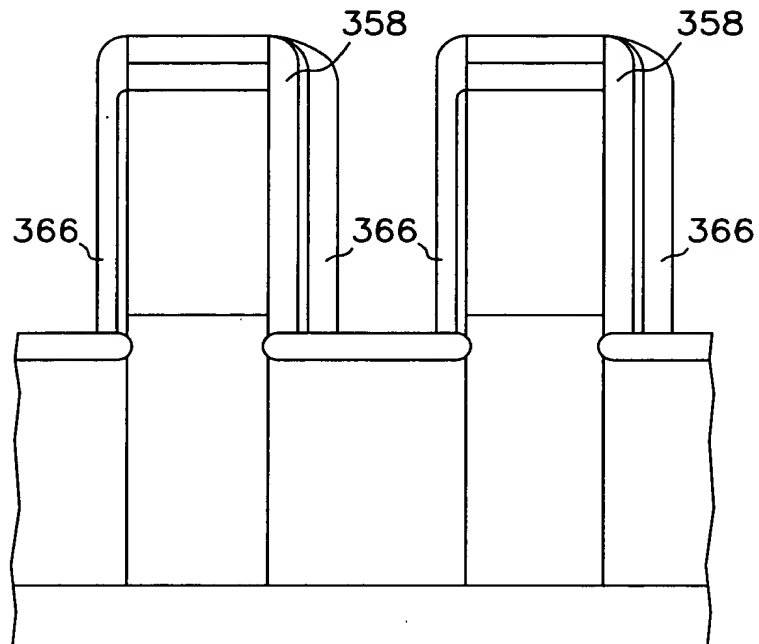
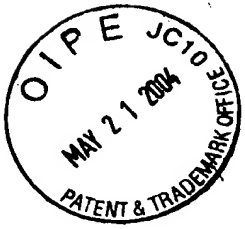


FIG. 5L



TITLE: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL
WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR
INVENTORS NAME: Wendell P. Noble Jr. et al.
SERIAL NO.: 09/551,027

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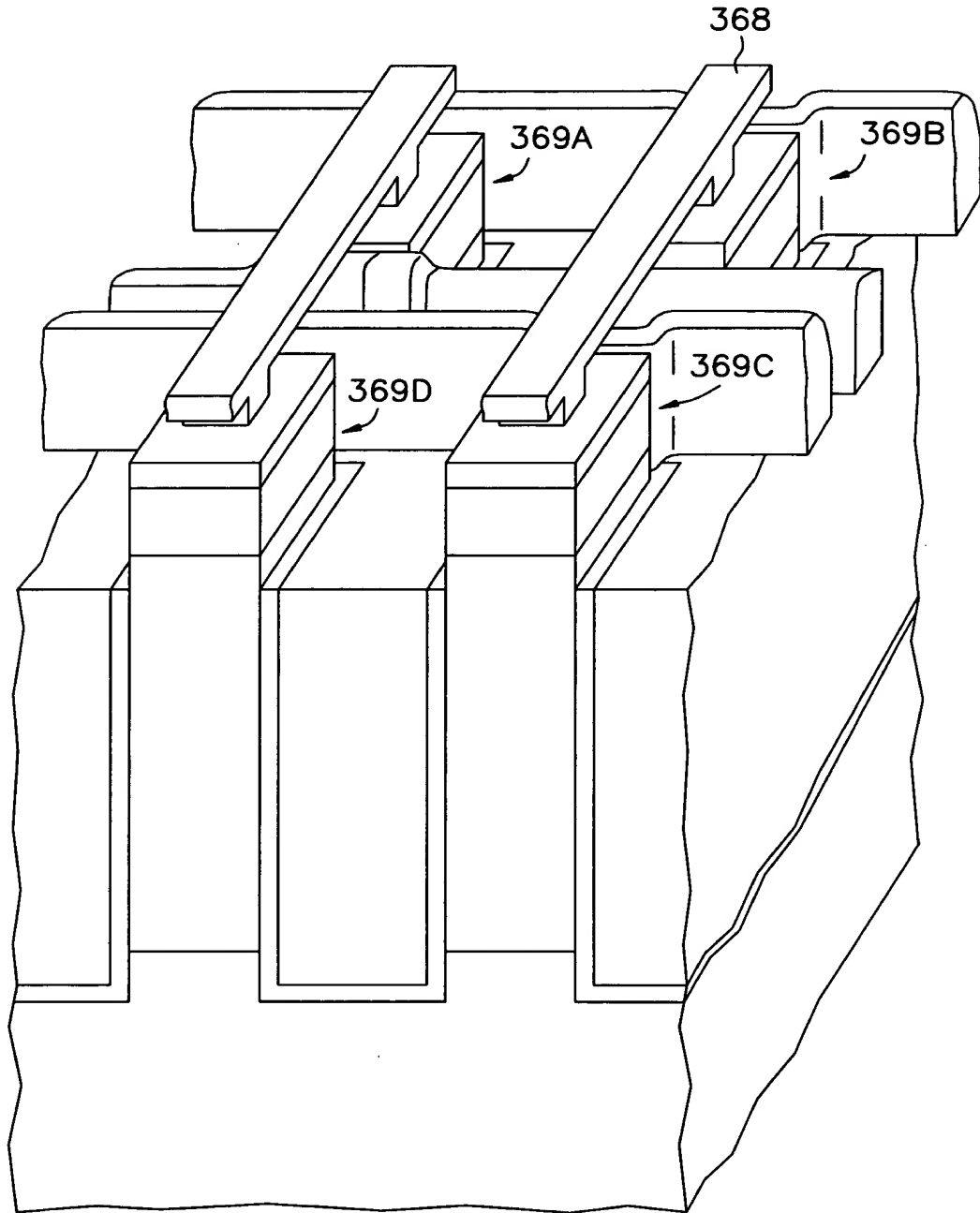


FIG. 5M